EUROSOI-ULIS 2026

PROGRAM

WEDNESDAY, 20th May 2026	
08:30 – 09:00	Registration and Welcome
09:00 – 09:40	**Invited Talk 1 - Tianchun Ye** **(Chinese Academy of Sciences)** **The Key Role of FD-SOI Technology in China** Chair: TBA
09:40 – 11:00	**SESSION 1 – RF and Millimeter-Wave Devices** Chair: TBA
09:40 – 10:00	**Can resistivity increase with doping?** Weijia Song (Université catholique de Louvain)
10:00 – 10:20	**Cryogenic RF Characterisation of Passive Components for VCO and PLL Design in P28 FD-SOI for Quantum Computing Applications** Victor Sabiá Pereira Carpes (CEA-Leti & Grenoble INP - CROMA)
10:20 – 10:40	**Role of Interface Degradation and Overlap Capacitance on the RF Performance of Self-Aligned Gate InGaAs MOSFETs** Mu Yu Chen (National Yang Ming Chiao Tung University)
10:40 – 11:00	**Opposite-Polarity Fixed Charges in BEOL Dielectrics for Interface Passivation on HR Silicon Substrates** Jingru Shen (Université catholique de Louvain)
11:00 – 11:30	Coffee Break
11:30 – 13:10	**SESSION 2 – FD-SOI Reliability** Chair: TBA
11:30 – 11:50	**BOX CREEP: A Mechanical Booster for Next-Generation FDSOI** Maxime Sauvagnac (CEA-LETI)
11:50 – 12:10	**Strain engineering of thin monocrystalline Si films on 8-inch wafers using Surface Activated Hot Bonding** Quentin Guillet (Univ. Grenoble Alpes, CEA-LETI)
12:10 – 12:30	**Impact of source/drain dopant implantation and spike annealing on electrical parameters of 25 nm FDSOI n-MOSFETs** Alexandre Vernhet (CEA / LETI)

12:30 – 12:50	**Impact of Device Position within the Silicon Active Area on Self-Heating and Thermal Coupling in FD-SOI Transistors** Nika Sahebghalam (Université catholique de Louvain)
12:50 – 13:10	**Analysis of uncertainties in the Self-Heating Extraction by RF technique in FD-SOI Transistors** Eric Vandermolen (ICTEAM, UCLouvain)
13:10 – 14:30	Lunch Break
14:30 – 15:10	**Invited Talk 2 - John Cressler (Georgia Tech)** **Using SiGe Electronics and Photonics in Space Systems** Chair: TBA
15:10 – 16:10	**SESSION 3 - Advanced Fabrication** Chair: TBA
15:10 – 15:30	**Mandrel material selection as prerequisite for SADP implementation at the 10 nm FD-SOI node** Sylvain Beaurepaire (Univ. Grenoble Alpes, CEA-Leti)
15:30 – 15:50	**Implantation- and Bonding-Free Multilayer SOI Fabrication via Annealing–Oxidation** Jungchul Lee (Korea Advanced Institute of Science and Technology)
15:50 – 16:10	**Fabrication and characterisation of GeSn devices for quantum applications** Nikolay Petkov (Munster Technological University and Tyndall National Institute)
16:10 – 16:40	Coffee Break
16:40 – 18:00	**SESSION 4 - Cryogenic Device Physics** Chair: TBA
16:40 – 17:00	**Impact of silicon thickness on the carrier mobility of 28 nm FDSOI MOSFET from room temperature to cryogenic regime** Jaime Calcade Rodrigues (Centro Universitário FEI)
17:00 – 17:20	**Demonstration of Trap Recovery by In-Situ Annealing in 28nm FD-SOI MOSFETs at Cryogenic Temperatures** Vincent Dieuzeide (ICTEAM Institute, Université catholique de Louvain)

17:20 – 17:40	**Cryogenic DC and Low-Frequency Noise Investigation of Vertical Gate-All-Around Silicon Nanowire pMOSFET Arrays** Abderrahim Tahiat (Normandie Univ, ENSICAEN, UNICAEN, CNRS, GREYC)
17:40 – 18:00	**Ultra-low threshold voltage shifts in passivated GaN-on-Si HEMTs under cryogenic operation** Siwei Zhou (University of Liverpool)
19:00 – 21:00	**Cultural Guided Tour**
21:00	**Welcome Cocktail at Carmen de la Victoria**

THURSDAY, 21st May 2026	
09:00 – 09:40	**Invited Talk 3 – Saptarshi Das (PennState)** **High-performance complementary 2D transistors and 3D integration for advanced logic** Chair: TBA
09:40 – 11:00	**SESSION 5 - 2D Materials** Chair: TBA
09:40 – 10:00	**Experimental Demonstration of 2D Core-Shell Junctionless FET** Mingyi Du (School of Electronic Science and Engineering, Nanjing University)
10:00 – 10:20	**In-depth TCAD study of stacked MoS_2 channel FETs based on a channel-last integration** Rihab Chouk (Univ. Grenoble Alpes, CEA, Leti)
10:20 – 10:40	**Ab-initio transport simulations of Dirac Source FETs based on van der Waals Heterojunctions between graphene and functionalized graphene** Khanh-Duy Nguyen (DPIA, University of Udine)
10:40 – 11:00	**DFT based layered dielectric model for MoS2/SiO2 structure** Ruben Ortega Lopez (University of Granda, CTIC UGR)

11:00 – 11:30	Coffee Break
11:30 – 13:10	**SESSION 6 - TCAD and beyond CMOS** Chair: TBA
11:30 – 11:50	**Forksheet versus Nanosheet Transistors: A Multi-Dimensional Scaling Comparison of Electrostatic Performance and Thermal Robustness** Diogo A. Vaccaro (LSI/PSI/USP, University of Sao Paulo)
11:50 – 12:10	**Impact of Forksheet Transistor on Low-Dropout Regulator Performance** Henrique De Mare Corazza (LSI/PSI/USP, University of Sao Paulo)
12:10 – 12:30	**Real Time Simulations of Advanced MOSFETs** Avanish Singh (IIT Hyderabad)
12:30 – 12:50	**Understanding room-temperature electrical characterizations of FDSOI spin qubit devices via TCAD simulations** Fatima Zahrae Tijent (Univ. Grenoble Alpes, CEA, Leti)
12:50 – 13:10	**Impact of RDF in the channel on the On-current of GAA nanosheet transistors through Monte Carlo simulations** Rhaycen Prates (Centro Universitário FEI)
13:10 – 14:30	Lunch Break
14:30 – 15:10	**Invited Talk 4 - Hanwool Yeon Gwangju (GIST)** **Synergistic Metallization Strategies for Heterogeneous Integration in Artificial Intelligence Hardware** Chair: TBA
15:10 – 16:30	**SESSION 7 - Contacts** Chair: TBA
15:10 – 15:30	**Reduced metal gate height and in-situ doped faceted raised source and drain regions for advanced RF FD-SOI devices** Yinyin Zhang Fu (CEA-Leti, UCLouvain)
15:30 – 15:50	**Low-temperature dielectric for BEOL integration of Si-based RFETs** Katrin Pingen (NaMLab gGmbH)

15:50 – 16:10	**ITO/TiW Contacts for Transparent FDSOI CMOS** Doga Selin Memikoglu (KTH Royal Institute of Technology, School of EECS)
16:10 – 16:30	**Contact Punch-Through Failure Mitigation in Advanced FD-SOI Nodes** Emmanuel Petitprez (Univ. Grenoble Alpes, CEA-Leti)
16:30 – 17:00	Coffee Break and **Poster Session** **(Poster details in Appendix I)**
17:00 – 19:00	**Poster Session** **(Poster details in Appendix I)**
21:00	**Gala Dinner at Hotel Gran Luna**

FRIDAY, 22nd May 2026	
09:00 – 09:40	**Invited Talk 5 - Andrea Capasso (INL)** **2D memristors for memory and neuromorphic applications** Chair: TBA
09:40 – 11:00	**SESSION 8 - Memristors, ReRAM** Chair: TBA
09:40 – 10:00	**Investigation of 1T1R Memristive Structures and Physics-Based Extension of the Stanford Model Including the Change of Filament Geometry** Nadine Dersch (THM University of Applied Sciences)
10:00 – 10:20	**Interface-Engineered Cryogenic Memristors Enabling Sub-100 µV Scalable Qubit Biasing** Erbing Hua (Delft University of Technology)
10:20 – 10:40	**Al-rich AlN thin films deposited by Molecular Beam Epitaxy on SiNx ReRAMs** Alexandros Eleftherios Mavropoulis (NCSR Demokritos)
10:40 – 11:00	**Improving the conductance ratio of mechanically-exfoliated MoS2 and WS2 based memristors** Deianira Fejzaj (Technische Universitaet Dresden)

11:00 – 11:30	Coffee Break
11:30 – 11:35	**FET 100 - Celebrating 100 years of the FET** Prof. Hiroshi Iwai (Eminent Lecturer of IEEE EDS)
11:35 – 13:15	**SESSION 9 - Emerging Devices (FET 100 - Celebrating 100 years of the FET)** Chair: Prof. Hiroshi Iwai
11:35 – 11:55	**The Ultimate Field Effect Transistor: GAIA MOSFET** Francis Balestra (Grenoble INP-CNRS)
11:55 – 12:15	**Enhancing Negative Differential Transconductance by Ultra-Thin Ge on SOI** Andreas Fuchsberger (Institute of Solid State Electronics, TU Wien)
12:15 – 12:35	**Split MLP Architectures for Accurate Joint Modeling of drain and gate currents in FD-SOI Transistors** Yusra Rachidi (CEA-LETI)
12:35 – 12:55	**From FD-SOI to MoS2 MOSFETs: Coupling Mechanisms** Xuan Zhang (GIICS Guangdong Greater Bay Area Institute of Integrated Circuit and System / Nanjing Universit)
12:55 – 13:15	**Single Trap and Low Frequency 1/f Noise Modeling in MOSFETs with Dirac Materials or 2D Semiconductor Channel** Pierpaolo Palestri (University of Modena and Reggio Emilia)
13:15 – 14:30	Lunch Break
14:30 – 16:10	**SESSION 10 - Emerging Memory Technologies** Chair: TBA
14:30 – 14:50	**Brain-Inspired Computing Enabled by a Universal NbOx Memristor with Multi-Mode Switching** Sungjun Kim (Dongguk University)
14:50 – 15:10	**Ultra-low-power in-memory computing based on spin-orbit ferroelectric devices for artificial intelligence and logic** Emanuel Vazquez (Spintec, UGA, CEA, CNRS)
15:10 – 15:30	**Ultra-low power Ru/TiOx/TiN RRAM structures for applications in neuromorphic computing** Piotr Jeżak (Warsaw University of Technology)

15:30 – 15:50	**Positive-Bias Erase Schemes for FeFETs: Switching Comparison Between FDSOI and Bulk devices** Dominik Martin Kleimaier (GlobalFoundries)
15:50 – 16:10	**Probabilistic bits based on Ag/SiOx/BE threshold switching memristors** Piotr Wiśniewski (Warsaw University of Technology)
16:10 – 16:40	Closing Remarks
16:40 – 17:10	Coffee Break

Appendix I

16:30 – 19:00	Poster Session
	P1: Analysis and Optimization of a Planar SOI RFET for Dynamic Reconfigurable Logic João Antonio Martino (Universidade de São Paulo (USP)
	P2: VTH Extraction in VGT-Normalized AlGaN/GaN HEMTs Maria Glória Caño de Andrade (São Paulo State University)
	P3: Vertical Capacitance and Edge-Field Engineering in 4H-SiC MOS Capacitors Maria Gloria Cano de Andrade (São Paulo State University (UNESP), Institute of Science and Technology)
	P4: Relocating Dopants from Si to SiO2: About Fundamentals and Applications of Modulation Acceptor Doping of Silicon Daniel Hiller (IAP Technical University Bergakademie Freiberg)
	P5: Simulating the Impact of Activation Functions on the Performance of 1T1R RRAM-Based Neural Networks Under Cycle-to-Cycle Variability Conditions Alan Blumenstein (THM University of Applied Sciences)
	P6: Enhancing High-Temperature Analog Performance of MOSFETs Through a Half-Diamond Layout Hardness-by-Design Approach Salvador Gimenez (FEI University Center)
	P7: A Scalable Time-Multiplexed Biasing Architecture for FDSOI Spin Qubits Antoine Faurie (CEA/LETI)

	P8: Co-Integration of Tunnel FET and FinFET for Hybrid LDO Circuit Design Pedro Henrique Madeira (FESJ-Unesp)
	P9: Study of Variability in Threshold Voltage Engineering for Nanosheet MOSFETs using TCAD Zih Fei Chen (Institute of Microelectronics Engineering, National Cheng Kung University)
	P10: Strategic Stress Engineering in CFETs: Monolithic vs. Sequential Ah-young Kim (Samsung Electronics & Sungkyunkwan University)
	P11: Al/SnO2/ITO-Based Memristive Soft-Threshold Neuron (MSTN) for Low-Power Neuromorphic Computing Partha Das (Svnit surat)
	P12: A T-Shaped Nanocavity Junctionless FET for High-Sensitivity Biomolecule Detection in Medical Diagnostics Mahsa Mehrad (University of Portsmouth)
	P13: Bias-dependent contact resistance model in Graphene on-Insulator FETs Nikolaos Mavredakis (Universitat Autònoma de Barcelona)
	P14: Feasibility Study of a Damage- and Pressure-Free AC Pseudo-MOS Method Using a Mercury Probe Ruka Yokoyama (Faculty of Engineering Science, Kansai University)
	P15: Optimization of Hybrid Source and Drain Extension Metal in AlGaN/GaN HEMTs: A Simulation and Experimental Study Howie Tseng (National Yang Ming Chiao Tung University, and Universidad de Granada)
	P16: High-precision Triboelectric Haptic Sensor for IoMT Healthcare Ethan Ahn (George Mason University)
	P17: Electrostrictive 2D Heterostructures for Steep Slope FET Applications Ethan Ahn (George Mason University)

	P18: Impact of Random Dopant Fluctuation in Stacked Drain Extended NSFETs Abhishek Acharya (S. V. National Institute of Technology Surat India)
	P19: Performance Assessment of Spacer Engineered InGaAs NSFETs: A Physical Insight Abhishek Acharya (S. V. National Institute of Technology Surat India)
	P20: Physical Electro-thermal Modelling of HfO2-based Nanoscale Memristor for Artificial Synapses Ankit Dixit (James Watt School of Engineering, University of Glasgow)
	P21: Properties of Ru/Hf1-xZrxO2/p-Si MOS Gate Stack Structures Deposited by Pulsed-DC Sputtering Using a Periodic Layer-by-Layer Deposition Process Rezwana Sultana (Warsaw University of Technology, Institute of Microelectronics and Optoelectronics)
	P22: Area-Dependent Switching and Synaptic Behavior in Al/TiOx/TiN devices Karimul Islam (Warsaw University of Technology, Institute of Microelectronics and Optoelectronics)
	P23: Mixed Finite Element Method for Quantum Dots Array Simulation Yingjia Gao (University of Glasgow)
	P24: Electric Field Control of Metal-to-Semiconductor Transition in BL-PtTe2 Sharieh Jamalzadeh Kheirabadi (Tyndall National Institute, University College Cork)
	P25: Experimental Nanosheet Transistors: Temperature and Inversion-Regime Effects on a Two-Stage Operational Transconductance Amplifier Thainá Guimarães (University of Sao Paulo)
	P26: Impact of Vertical Nanowire VFET Structural Asymmetry on Static and Dynamic Performance of Two-Stage OTA Paula Agopian (UNESP - Sao Paulo State University)

	P27: Unified Physics-Based Verilog-A Compact Model of Independent-Gate Reconfigurable FETs: Dual- and Triple-Gate Architectures Ananya Karmakar (THM University of Applied Sciences)
	P28: Interplay of Hot Carrier Degradation and Device Variability in NSFETs: A TCAD Study Naveen Kumar (James Watt School of Engineering, University of Glasgow)
	P29: Electronic Structure of W-doped In2O3 BEOL Oxide Semiconductors John Robertson (Cambridge University)
	P30: Absence of P-doping by Localized Acceptor Polarons in TeO2 Semiconductors John Robertson (Cambridge University)
	P31: Band gap and Defects of AlScN ferroelectrics for BEOL non-volatile memories Ruyue Cao (Cambridge University)
	P32: Electronic Structure of IGZO and its Hydrogen Defects Ruyue Cao (Cambridge University)
	P33: Origin of ferroelectricity in HfO2/ZrO2 thin films without depolarization Ruyue Cao (University of Cambridge)
	P34: Temperature Influence on Single Trap Junctionless Nanowire Transistors Low-Frequency Noise Rodrigo Doria (Centro Universitário FEI)
	P35: Orientation-engineered PtTe2 Schottky FETs for dopant-free advanced technology nodes Farzan Gity (Tyndall National Institute, University College Cork)
	P36: Tuning the metal-insulator transition in ultrathin silicon-on-insulator films through interface engineering Andrea Pulici (CNR-IMM, Unit of Agrate Brianza)

	P37: Experimental Emulation and Functional Validation of a Dual-Doped Reconfigurable FET for Hardware Security Antonio Manuel Hervas Ramirez (CITIC UGR)
	P38: On the activation of dopants in ultrathin Si films: interface effects and dielectric mismatch at work Michele Perego (CNR-IMM)
	P39: Stack-in-Pillar, a CFET strategy to implement IC at advanced technology nodes Hugo Lozano (Institute of Microelectronics of Barcelona)
	P40: A compact model of perovskite memristors inspired by the Stanford RRAM model Bitania Shiferaw Mengesha (Universitat Rovira i Virgili)
	P41: DC characterization of BEOL metallic layers in silicon technologies for cryogenic microelectronics Stanislas Pastor (STMicroelectronics / Université Grenoble Alpes - TIMA / Université de Sherbrooke - Institut Quantique)
	P42: SOI based Nanowire Field-Effect Transistor Biosensors with Diamond-Like Carbon Modification Hanlin Long (Forschungszentrum Jülich GmbH)
	P43: Exploiting SOI nonlinear heterogeneity to implement KAN physical networks using Synaptic Nonlinear Elements Marco Fanciulli (University of Torino)
	P44: Temperature Dependent Carrier Transport Mechanisms in WSe2 Stephen O'Sullivan (MicroNano systems, Tyndall National Institute, University College Cork)
	P45: Analytical Modeling of Rectifiers for Radio-Frequency Energy Harvesting Renan Trevisoli (PUC - SP)

	P46: Impact of neglecting the bias dependence of access resistances on DC and 1/f noise parameter extraction Bogdan Cretu (Normandie Univ, ENSICAEN, UNICAEN, CNRS, GREYC)
	P47: Non-Quasi Static Small Signal Model of a Nanosheet FET for High-Frequency Application: Capturing the Role of the Corner Rounding Sandeep Kumar (Indian Institute of Technology Bhubaneswar)
	P48: Demonstration of the Novel Junctionless Complementary FET Sandeep Kumar (Indian Institute of Technology Bhubaneswar)
	P49: Analysis of Self Heating in SiC-6H and Al2O3 Substrate Platforms with SiO2 Buried Oxide Integration on AlGaN HEMT Pankaj Kumar (Dhirubhai Ambani University)
	P50: Impact of BOX scaling and ground plane on 1/f noise in FDSOI pMOSFET Prabhat Khedgarkar (Indian Institute of Technology Ropar)
	P51: Optimization of Magnetron-Sputtered Al Thin Films for Controlled Surface Roughness in RRAM Applications Michał Jarosik (Warsaw University of Technology, Centre for Advanced Materials and Technologies CEZAMAT)
	P52: Dielectric BD in FDSOI Transistors: circuital compact model and Impact on digital Circuits Rishab Goyal (Autonoma University of Barcelona)
	P53: Statistical Robustness Analysis of Diamond MOSFETs under High-Dose Gamma Radiation in 350 nm Bulk CMOS Technology Vinicius Vono Peruzzi (CTI Renato Archer)
	P54: Statistical Robustness Analysis of MOSFETs with Different Layout Styles Under Gamma Radiation Using the Coefficient of Variation Vinicius Vono Peruzzi (CTI Renato Archer)

	P55: Study of the annealing effect on Al2O3-based 1T1R RRAM cell Aleksander Malkowski (Warsaw University of Technology, Center for Advanced Materials and Technology CEZAMAT)
	P56: Operation of Junctionless Nanowire Transistors-Based Common Source Current Mirror at Cryogenic Temperatures Rodrigo Trevisoli Doria (Centro Universitário FEI)